Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Previously presented) A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal x(t), emulating the mixing of said input signal x(t) with a local oscillator signal having frequency *f*, said synthesizer comprising:

a first signal generator for producing a first mixing signal $\phi 1$, which varies irregularly over time; and

a second signal generator for producing a second mixing signal $\phi 2$ which varies irregularly over time;

where:

$\phi 1 * \phi 2$ has significant power at the frequency *f* of said local oscillator signal being emulated;

neither $\phi 1$ nor $\phi 2$ has significant power at the frequency *f* of said local oscillator signal being emulated, and

said mixing signals $\phi 1$ and $\phi 2$ are designed to emulate said local oscillator signal having frequency *f*, in a time domain analysis.

2. (Previously presented) The synthesizer of claim 1, wherein signals used to generate $\phi 1$ and $\phi 2$ do not have a significant amount of power at the frequency designed to be output from said successive mixers in ~~of said~~ output signal x(t) $\phi 1$ $\phi 2$.

3. (Previously presented) The synthesizer of claim 2, wherein $\phi 1 * \phi 1 * \phi 2$ does not have a significant amount of power within the bandwidth designed to be output from said successive mixers, in said output signal x(t) $\phi 1$ $\phi 2$.

4. (Previously presented) The synthesizer of claim 3, wherein $\phi 2 * \phi 2$ does not have a significant amount of power within the bandwidth designed to be output from said successive mixers in said output signal x(t) $\phi 1$ $\phi 2$.

5. (Previously presented) The synthesizer of claim 4, wherein said first and second mixing signals $\phi 1$ and $\phi 2$ are generated using a single time base.

6. (Previously presented) The synthesizer of claim 4, wherein said first and second mixing signals $\phi 1$ and $\phi 2$ are digital waveforms.

7. (Previously presented) The synthesizer of claim 4, wherein said first and second mixing signals $\phi 1$ and $\phi 2$ are square waveforms.

8. (Previously presented) The synthesizer of claim 4, wherein said mixing signal $\phi 2$ is a square wave.

9. (Previously presented) The synthesizer of claim 4, wherein said mixing signals $\phi 1$ and $\phi 2$ effect the mixing of an in-phase component of said input signal x(t), and a complementary pair of successive mixers with mixing signals 90 degrees out of phase, are used to effect the modulation of a quadrature component of said input signal x(t).

10. (Previously presented) The synthesizer of claim 4, wherein said first and second mixing signals $\phi 1$ and $\phi 2$ are periodic functions of time.

11. (Previously presented) The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first mixing signal $\phi 1$; and complementary means for generating said second mixing signal $\phi 2$.

12. (Previously presented) The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal S; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first mixing signal $\phi 1$.

13. (Previously presented) The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal S to be synchronized in time with said first mixing signal $\phi 1$, outputting said delayed control signal S as said second mixing signal $\phi 2$.

14. (Previously presented) The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second mixing signals $\phi 1$ and $\phi 2$ by shifting out corresponding predetermined sequences.

15. (Previously presented) The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal $\phi 1$, by shifting out a predetermined sequence.

16. (Previously presented) The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register, and

a second shift register being clocked by said XOR output, and generating said second mixing signal $\phi 2$, by shifting out a second predetermined sequence.

17. (Previously presented) The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second mixing signal $\phi 2$, by shifting out a predetermined sequence.

18. (Previously presented) The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first mixing signal $\phi 1$, from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal S having edges aligned with said oscillator signal; and

means for delaying said control signal S to produce said second mixing signal $\phi 2$.

19. (Previously presented) The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal S at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal S to produce said second mixing signal $\phi 2$.

20. (Previously presented) The synthesizer of claim 19, wherein said means for generating said first mixing signal $\phi 1$, comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal x(t), producing said first mixing signal $\phi 1$.

21. (Original) The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. (Previously presented) The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal $\phi 1$, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first mixing signal $\phi 1$, and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. (Previously presented) The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional mixing signals, varying irregularly over time;

where the product of all of said mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said mixing signals has significant power at the frequency of said local oscillator signal being emulated.

24. (Previously presented) The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first mixing signal $\phi 1$.

25-26. Canceled.

27. (Previously presented) The synthesizer of claim 12, wherein said control signal S comprises a periodic signal.

28. (Previously presented) The synthesizer of claim 12, comprising:

a delta-sigma (Δ-S) modulator for generating said control signal S.

29. (Previously presented) The synthesizer of claim 4 comprising:

first and second latches which are clocked via a common clock, to align said first and second mixing signals $\phi 1$ and $\phi 2$.

30. (Previously presented) An integrated circuit comprising the synthesizer of claim 1.

31-32. Canceled.

33. (Previously presented) The synthesizer of claim 4, wherein the patterns of said first and second mixing signals $\phi 1$ and $\phi 2$ are different from one another.